V R SIDDHARTHA ENGINEERING COLLEGE
(AUTONOMOUS)
VIJAYAWADA

Date: 13/06/2024

NOTICE

The Semester-end Examination of B.Tech., IV-Semester (VR20) Regular & Supplementary Examinations for the following subjects is rescheduled as given below.

Subject Code & Name	Actual Schedule of Examination & Date & Time	Postponement of Examination & Date & Time
IV-Semester 20AI&DS4302 / 20AI&ML4302 Design & Analysis of Algorithms **(AI&DS/AI&ML)** 20CE4302-Structural Analysis 20CS4302-Advanced Data Structures & Algorithms 20ES4102-Control Systems**(ECE)** 20EE4302-Linear Control Systems 20EI4302-Linear Integrated Circuits & Applications**(EIE)** 20IT4302-Java Programming 20ES4102A-Electrical & Electronics Engineering **(ME)**	12/06/2024 Wednesday (9.00AM to 12.00 Noon)	28/06/2024 Friday (9.00AM to 12.00 Noon)

Students are advised to note the change in the time-table and attend the semester end examinations accordingly.

(Dr. T S R CHOWDARY)
Dy. Controller of Examinations

(Dr. A V RATNA PRASAD)
Principal

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