

V R SIDDHARTHA ENGINEERING COLLEGE
(AUTONOMOUS)
VIJAYAWADA


Date: 12/11/2022


NOTICE

The Semester-end Examination of B.Tech., VII-Semester (VR17) Regular & Supplementary Examinations for the following subjects is rescheduled as given below.

Subject Code & Name	Actual Schedule of Examination & Date & Time	Postponement of Examination Date & Time
17CS4702A – Data Analytics 17EC4702B – Optical Communication 17EC4702C – Principles of Radar Engineering 17EC4702D – Adhoc & Sensor Networks 17EE4702C – High Voltage Engineering 17EE4702D – Optimization Techniques 17EI4702A – Power Plant Instrumentation 17EI4702D – Drives & Control for Industrial Automation	16/11/2022 Wednesday (2.00 PM to 5.00 PM)	28/11/2022 Monday (2.00 PM to 5.00 PM)

Students are advised to note the change in the time-table and attend the semester end examinations accordingly.


(Dr. T S R CHOWDARY)
Dy. Controller of Examinations


(Dr. A V RATNA PRASAD)
Principal

To
All Notice Boards
Web site
Exam Section